



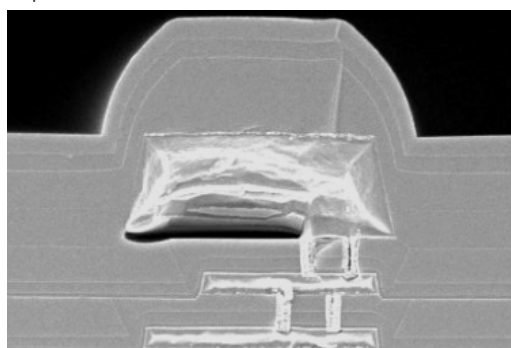
CMOS14P 5V Power process: A-Gate (process freeze) achieved

We are delighted to inform you that CMOS14 5V Power process has reached the milestone of A-Gate (Process freeze) on 27 Mar 2009 in SSMC. The development of this process is being done by various groups in NXP (Front End Innovation/PIFIT, PLT and various Business lines) together with SSMC.

This achievement allows us to support customer with specific process requirement for power management applications, such as high speed interface, display port adapter. CMOS14P provide very thick M5 as the top metal is specially designed to support the power device needs (see Fig. 1). Process capability and technical feasibility have been evaluated, see typical 5V transistor in Table 1 below.

Fig.1 Cross-section view of critical structure

Top Thick Metal over normal metal beneath



HIGHLIGHTS

- First silicon from prototype lot is functional
- CMOS14P 5V V-Gate and R-Gate are expected in ww938 and ww951 respectively.
- Currently, we are also qualifying CMOS14P 20V process. We expect A-Gate in ww925
- For more information on CMOS14P process option, please contact our account managers or email to marketing@ssmc.com

Table 1 Typical 5V transistor data

Typical 5V transistor data		5V NMOS		5V PMOS	
Parameter	Unit	Spec	Meas	Spec	Meas
BVdss @ Jds=1nA/um	V	>8	8.3-10	>8	8.3-8.9
Ron*area @ Vgs=2.3 V	mOhm mm2	<4.2	4.3	<13	13
Ron*area @ Vgs=5.0 V	mOhm mm2		2.1		5.5
Vth	V	<0.75	0.63	<0.75	0.75
Jleak @ Vds=5.5 V	pA/um	<0.5	0.5	< 0.5	2